**Test Case #1: 22 points**

| 4000 | I0 | MOVC R1,#10 |
| --- | --- | --- |
| 4004 | I1 | MOVC R5,#45 |
| 4008 | I2 | MOVC R10,#230 |
| 4012 | I3 | ADD R6,R10,R5 |
| 4016 | I4 | MOVC R13,#20 |
| 4020 | I5 | SUB R12,R10,R6 |
| 4024 | I6 | SUBL R12,R6,#10 |
| 4028 | I7 | STORE R6,R1,#22 |
| 4032 | I8 | LOAD R14,R13,#12 |
| 4036 | I9 | MOVC R0,#12 |
| 4040 | I10 | MOVC R8,#22 |
| 4044 | I11 | STR R13,R13,R1 |
| 4048 | I12 | MUL R10,R0,R8 |
| 4052 | I13 | AND R1,R10,R14 |
| 4056 | I14 | HALT |
| 4060 | I15 | EX-OR R10,R12,R13 |
| 4064 | I16 | LDR R6,R13,R0 |
| 4068 | I17 | MOVC R12,#10 |
| 4072 | I18 | AND R8,R6,R5 |
| 4076 | I19 | SUB R6,R0,R14 |

2 points per correct value

| R0 | 12 |  | D30 | 20 |
| --- | --- | --- | --- | --- |
| R1 | 256 |  | D32 | 275 |
| R2 |  |  |  |  |
| R3 |  |  |  |  |
| R4 |  |  |  |  |
| R5 | 45 |  |  |  |
| R6 | 275 |  |  |  |
| R7 |  |  |  |  |
| R8 | 22 |  |  |  |
| R9 |  |  |  |  |
| R10 | 264 |  |  |  |
| R11 |  |  |  |  |
| R12 | 265 |  |  |  |
| R13 | 20 |  |  |  |
| R14 | 275 |  |  |  |
| R15 |  |  |  |  |

**Test Case #2: 20 points**

| 4000 | I0 | MOVC,R0,#2 |
| --- | --- | --- |
| 4004 | I1 | MOVC,R1,#8 |
| 4008 | I2 | MOVC,R2,#4 |
| 4012 | I3 | MOVC,R3,#1 |
| 4016 | I4 | MOVC,R4,#4 |
| 4020 | I5 | STORE,R0,R2,#0 |
| 4024 | I6 | ADD,R2,R2,R4 |
| 4028 | I7 | SUBL,R1,R1,#0 |
| 4032 | I8 | CMP,R2,R1 |
| 4036 | I9 | BZ,#-16 |
| 4040 | I10 | MOVC,R0,#0 |
| 4044 | I11 | MOVC,R1,#8 |
| 4048 | I12 | MOVC,R2,#4 |
| 4052 | I13 | LOAD,R5,R2,#0 |
| 4056 | I14 | ADD,R5,R5,R0 |
| 4060 | I15 | ADD,R0,R0,R3 |
| 4064 | I16 | STORE,R5,R2,#0 |
| 4068 | I17 | ADD,R2,R2,R4 |
| 4072 | I18 | SUB,R1,R1,R3 |
| 4076 | I19 | CMP,R0,R1 |
| 4080 | I20 | BNZ,#-28 |
| 4086 | I21 | HALT, |
| 4090 | I22 | MOVC,R3,#10 |

2 points per correct value

| R0 | 4 |  | D[4] | 2 |
| --- | --- | --- | --- | --- |
| R1 | 4 |  | D[8] | 3 |
| R2 | 20 |  | D[12] | 2 |
| R3 | 1 |  | D[16] | 3 |
| R4 | 4 |  |  |  |
| R5 | 3 |  |  |  |

Test case 3:

(I0) 4000 MOVC R0,#-4

(I1) 4004 MOVC R1,#1

(I2) 4008 MOVC R1,#0

(I3) 4012 MOVC R2,#2

(I4) 4016 MOVC R15,#4000

(I5) 4020 MOVC R14,#68

(I6) 4024 MOVC R3,#0

(I7) 4028 SUB R4,R2,R3

(I8) 4032 BZ #16

(I9) 4036 JALR R5,R14,#4000

(I10) 4040 ADDL R3,R3,#1

(I11) 4044 JUMP R15,#28

(I12) 4048 MUL R1,R1,R2

(I13) 4052 LOAD R5,R0,#0

(I14) 4056 MUL R1,R1,R2

(I15) 4060 HALT

(I16) 4064 MOVC R2,#1000

(I17) 4068 ADDL R1,R1,#4

(I18) 4072 STORE R1,R0,#4

(I19) 4076 ADDL R0,R0,#4

(I20) 4080 RET R5

(I21) 4084 MOVC R0, #10

(I22) 4088 MOVC R0, #10

(I23) 4088 MOVC R0, #10

(I24) 4088 MOVC R0, #10

(I25) 4088 MOVC R0, #10

**Test Case #3: 75 points**

| **#No.** | **Cycle #** | **Description** | **Points** |
| --- | --- | --- | --- |
| 0 | 8 | Check the ROB retirement.   * I0 is committed in cycle 7. * Check the architecture RF in cycle 8 | 2 |
| 1 | 11 | Check if most recent physical CC is updated in rename table.  (Timing: Next cycle after I7 in RD2.) | 3 |
| 2 | 12 | Correct only one branch in pipeline (Timing: After dispatch of I8.)  Check if I9 is stalled 5 cycles in the DR1.  (Timing: After I9 in DR1.) | 5 |
| 3 | 21 | Correct BTB implementation (Timing: After JALR is in BU.)   * Check JALR (I9) if a correct instruction (I17) is fetched in cycle #21   (Timing: After I9 in BU.) | 3 |
| 4 | 18, 20,  22 | Correct implementation of JALR(I9).   * Check the physical register (P8) allocation in cycle 18. * Check the commitment of I9 in cycle 22.   (Timing: Next cycle after I9 in RD2.) | 5 |
| 5 | 25 | Correct implementation of LSQ.   * LSQ entry is created for I18.   (Timing: Next cycle after I18 in RD2.) | 5 |
| 6 | 26 | Check Store should not be stalled due to invalidation of src1.   * I18 should be issued in cycle 26 (I18 in IU).   (Timing: Two cycles after I18 in RD2.) | 2 |
| 7 | 26, 27 | Squash all instructions after RET (I20)   * Check I21 and I22 are squashed in cycle 26. * Check I10 is fetched in cycle 27.   (Timing: Two cycles after I20 in DR1.) | 5 |
| 8 | 32, 34 | Correct JUMP (I11) implementation   * Check all instructions are squashed after cycle 32. * Check I7 is fetched in cycle 34.   (Timing: Two cycles after I11 in BU.) | 5 |
| 9 | 37 | Correct BTB hit.   * I9 should hit in BTB. * I17 should be fetched in cycle 38.   (Timing: Next cycle after I9 in RD2.) | 5 |
| 10 | 59 | Check BTB update after I8 first TAKEN   * Check I12 is fetched in cycle 59.   (Timing: Two cycles after I8 in BU.) | 10 |
| 11 | 63-66 | Check Mul Unit has 4 cycles.  (Timing: Two cycles after I12 in RD2.) | 5 |
| 12 | 64 | Check free list implementation.   * P0 should be allocated in cycle 64 (I14).   (Timing: Next cycle after I14 in RD2.) | 3 |
| 13 | 69 | Check forwarding from MUL to MUL.   * Check I14 is executed in cycle 69 in the Mul unit.   (Timing: Two cycles after I12 in MU-Writeback.) | 5 |
| 14 | 75 | Check the HALT.   * Program should be ended in cycle 75. | 2 |
| 15 | 75 | Check STORE instruction.   * Check if mem[0]=4 and mem[4] = 8.   (Timing: In the end.) | 4 |
| 16 | 75 | Check Architecture RF values.  (Timing: In the end.) | 6 |